CYCLE #		BUS Ct1 4-				BUS	-BUS DATA [8:0]-	[8:0]——			\$H7
	0	START OP[0]	0P[0]			ΑD	ACDRESS [9:2]	[9:2]			
~~		OP[1] OP[3]	OP[3]			AD	ADDRESS	[17:10]		·	
	2	C/D				AD	ADDRESS	[26:18]			
	u	OP[2]				AD	ADDRESS [35:27]	[35:27]			
	4	C/D	M A	MASTER (3: 1)]	COUNT	COUNT [6,4,2]			RSRV	
	ഗ	RSRV	MΑ	MASTER [1:0]	·J	COUNT	COUNT [7,5,3]	COU	COUNT [1:0]	ADDRESS [1:0]	S [1:0]

FIGURE 4

One Byte Transfer (MasterCount[7:0] = 00000000)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4}	Mask[3:0]	Mask[7:4] end Mask[3:0]
200000000	00	00	0001	1111	0001
20000000	01 .	01	0011	1110	0010
20000000	10	10	0111	1100	0100
20000000	11	11	1111	1000	1000

FIGURE 7a

Two Byte Transfer (MasterCount[7:0] = 00000001)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4}	Mask[3:0]	Mask[7:4] and Mask[3:0]
<i>9</i> 0000000	01	00	0011	1111	0011
20000000	10	01	0111	1110	0110
200 00000	11	10	1111	1100	1100
£0000001	00	11	0001	1000	not used - two QB's

FIGURE 7b

Four Byte Transfer (MasterCount[7:0] = 00000011)

Gount[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
00000000	11	00	1111	1111	1111
90 000001	00	01	0001	1110	not used - two QB's
20000001	01	10	0011	1100	not used - two QB's
Q0000001	10	11	0111	1000	not used - two QB's

FIGURE 7c

Elght Byte Transfer (MasterCount[7:0] = 00000111)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4}	Mask[3:0]	Mask[7:4] and Mask[3:0]
9000001	11.	00	1111	1111	not used - two QB's
Ø000010	00	01 ·	0001	1110	not used - three QB's
9000010	01	10	0011	1100	not used - three QB's
90000010	10	11	0111	1000	not used - three QB'

FIGURE 7d